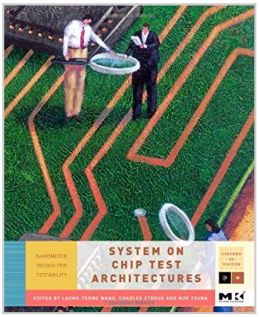

System-on-Chip Test Architectures, Volume .: Nanometer Design for Testability (Systems on Silicon)

By Laung-Terng Wang, Charles E. Stroud, Nur A. Touba

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Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost.

This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs.

- Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples.
- Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book.
- Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits.
- Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing.
- Practical problems at the end of each chapter for students.

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Editorial Review

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Laung-Terng Wang, Ph.D., is founder, chairman, and chief executive officer of SynTest Technologies, CA. He received his EE Ph.D. degree from Stanford University. A Fellow of the IEEE, he holds 18 U.S. Patents and 12 European Patents, and has co-authored/co-edited two internationally used DFT textbooks- VLSI Test Principles and Architectures (2006) and System-on-Chip Test Architectures (2007).

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